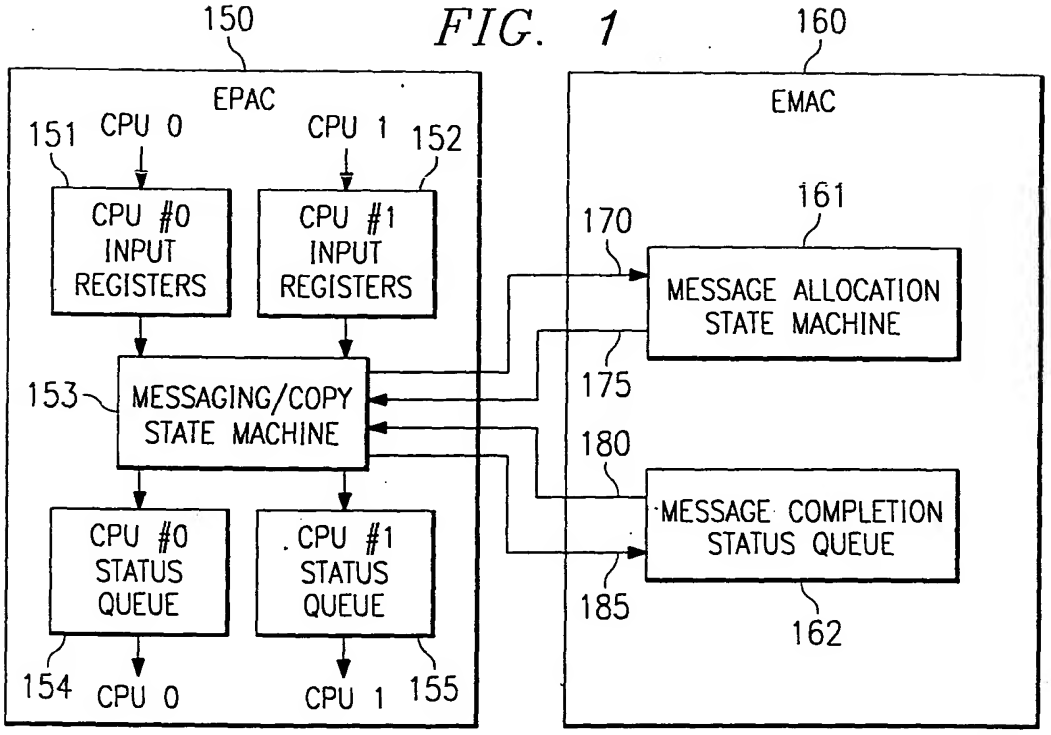
FIG. 1


150
EPAC
151
CPU 0
CPU 1
152
CPU #0 INPUT REGISTERS
CPU #1 INPUT REGISTERS
153
MESSAGING/COPY STATE MACHINE
CPU #0 STATUS QUEUE
CPU #1 STATUS QUEUE
154
CPU 0
CPU 1
155
160
EMAC
161
170
MESSAGE ALLOCATION STATE MACHINE
175
180
MESSAGE COMPLETION STATUS QUEUE
185
162

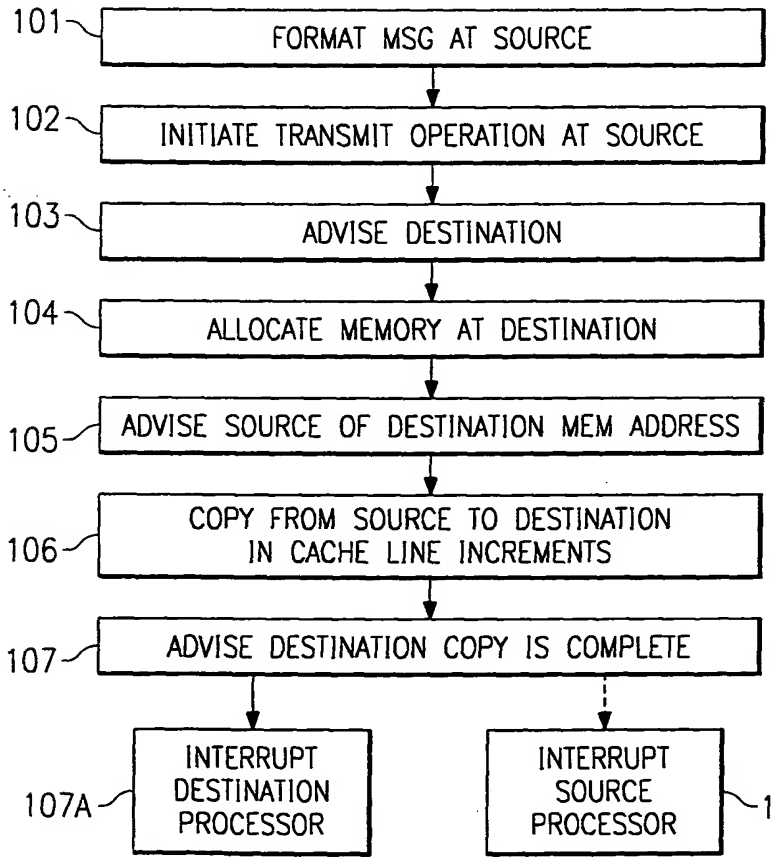

101
FORMAT MSG AT SOURCE
102
INITIATE TRANSMIT OPERATION AT SOURCE
103
ADVISE DESTINATION
104
ALLOCATE MEMORY AT DESTINATION
105
ADVISE SOURCE OF DESTINATION MEM ADDRESS
106
COPY FROM SOURCE TO DESTINATION IN CACHE LINE INCREMENTS
107
ADVISE DESTINATION COPY IS COMPLETE
107A
INTERRUPT DESTINATION PROCESSOR
INTERRUPT SOURCE PROCESSOR
107B

FIG. 1A

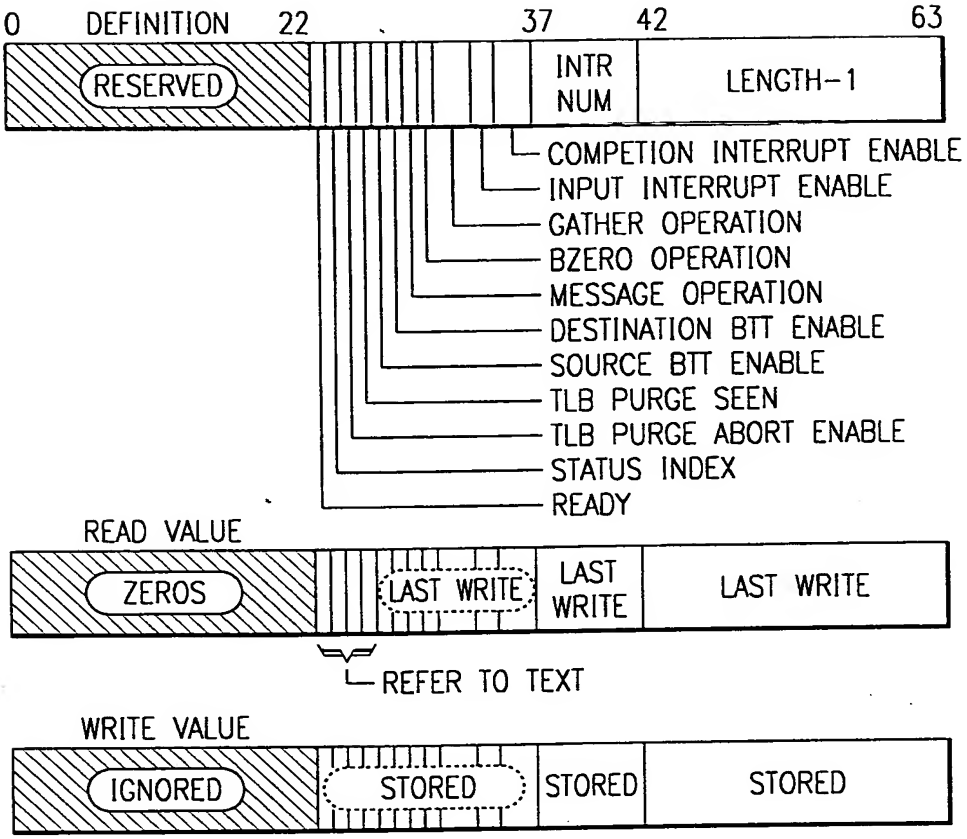

0
DEFINITION
22
37
42
63
RESERVED
INTR NUM
LENGTH-1
COMPETION INTERRUPT ENABLE
INPUT INTERRUPT ENABLE
GATHER OPERATION
BZERO OPERATION
MESSAGE OPERATION
DESTINATION BTT ENABLE
SOURCE BTT ENABLE
TLB PURGE SEEN
TLB PURGE ABORT ENABLE
STATUS INDEX
READY
READ VALUE
ZEROS
LAST WRITE
LAST WRITE
LAST WRITE
REFER TO TEXT
WRITE VALUE
IGNORED
STORED
STORED
STORED

FIG. 2

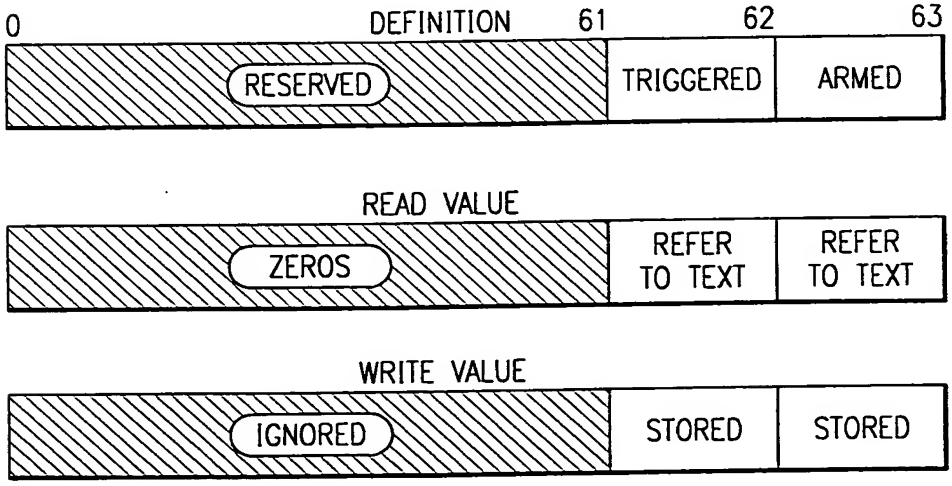

0
DEFINITION
61
62
63
RESERVED
TRIGGERED
ARMED
READ VALUE
ZEROS
REFER TO TEXT
REFER TO TEXT
WRITE VALUE
IGNORED
STORED
STORED

FIG. 2A

FIG. 3

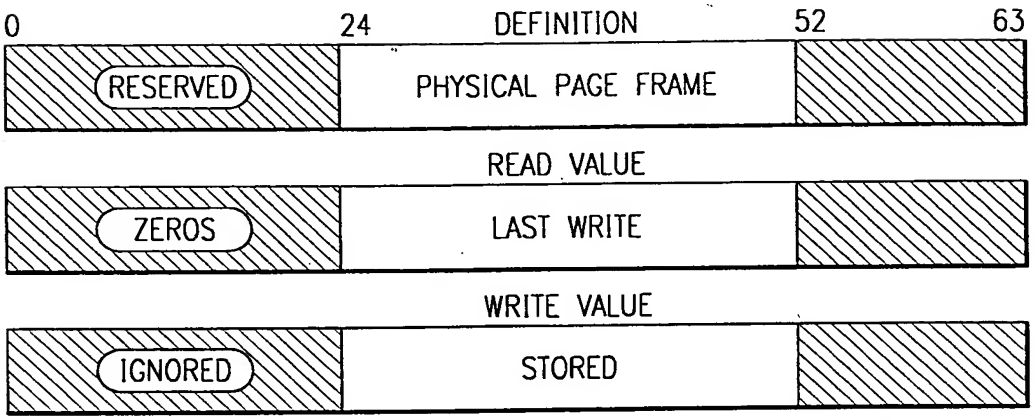


FIG. 4

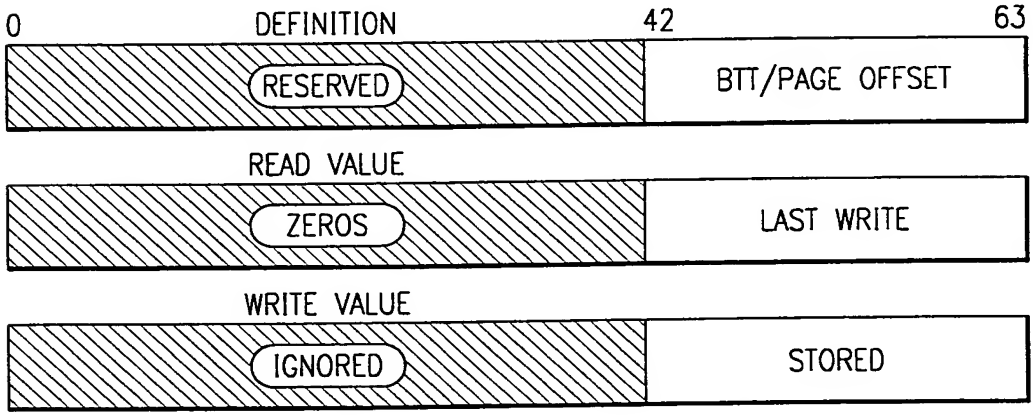


FIG. 5

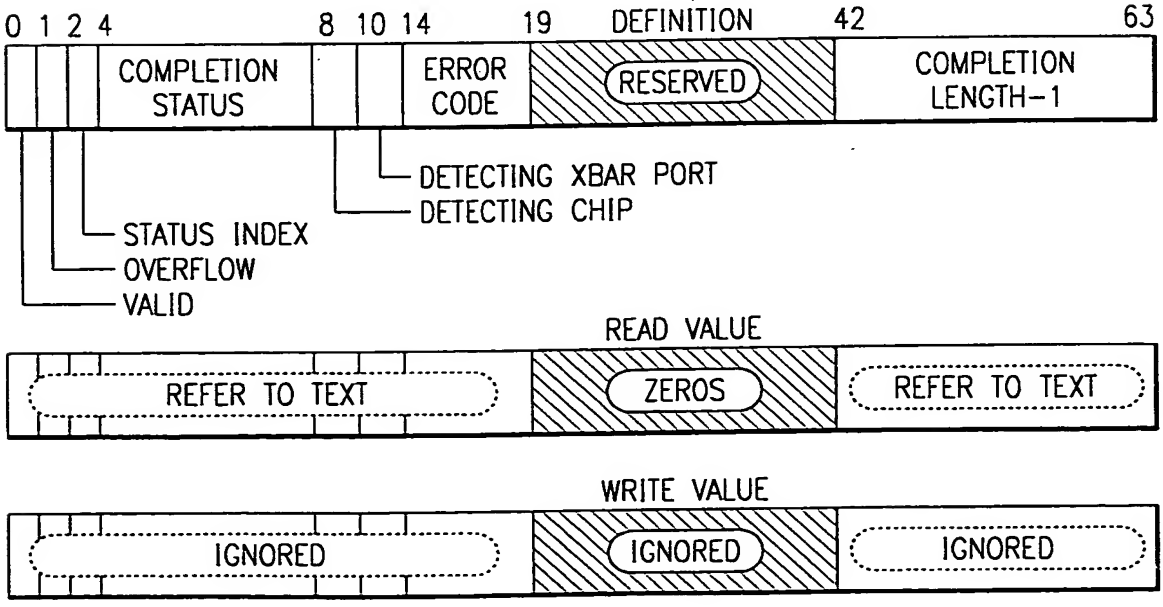


FIG. 6

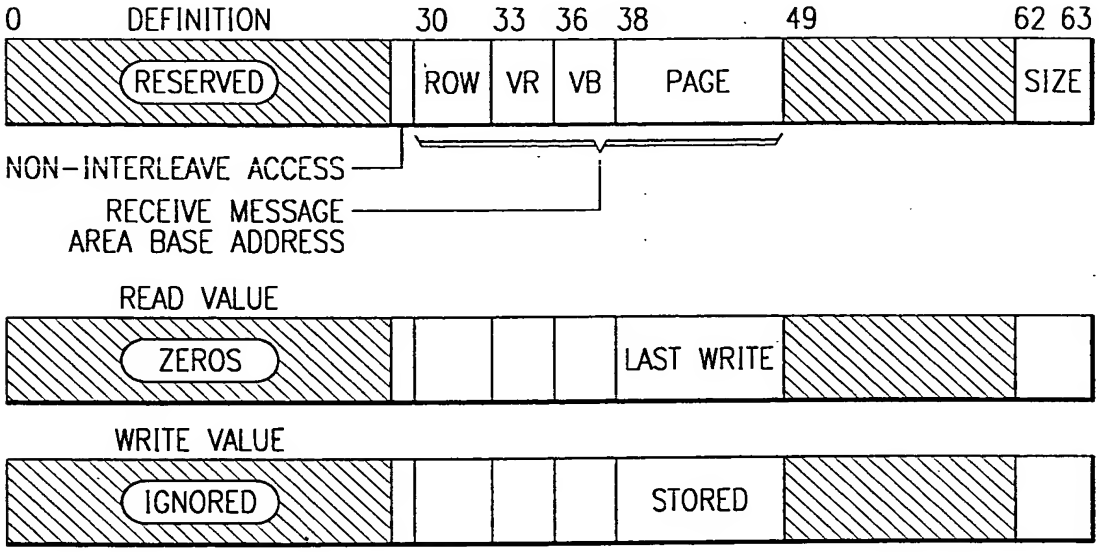


FIG. 7

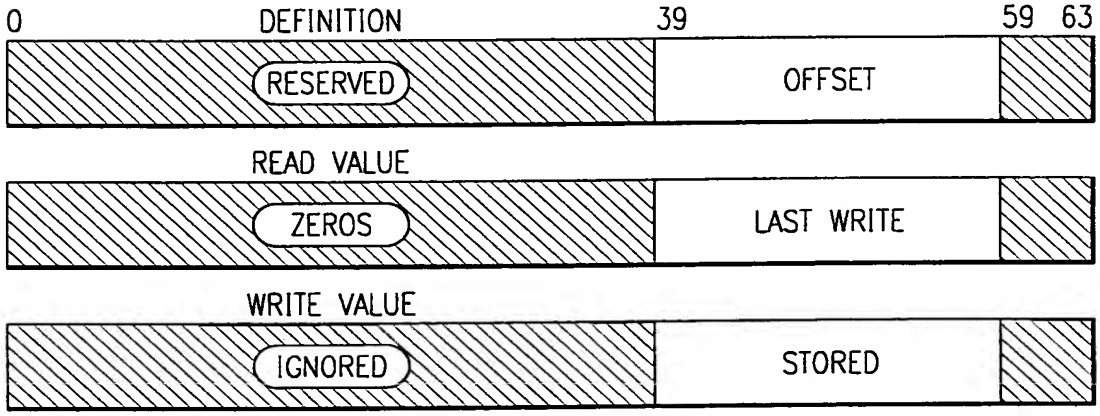


FIG. 8

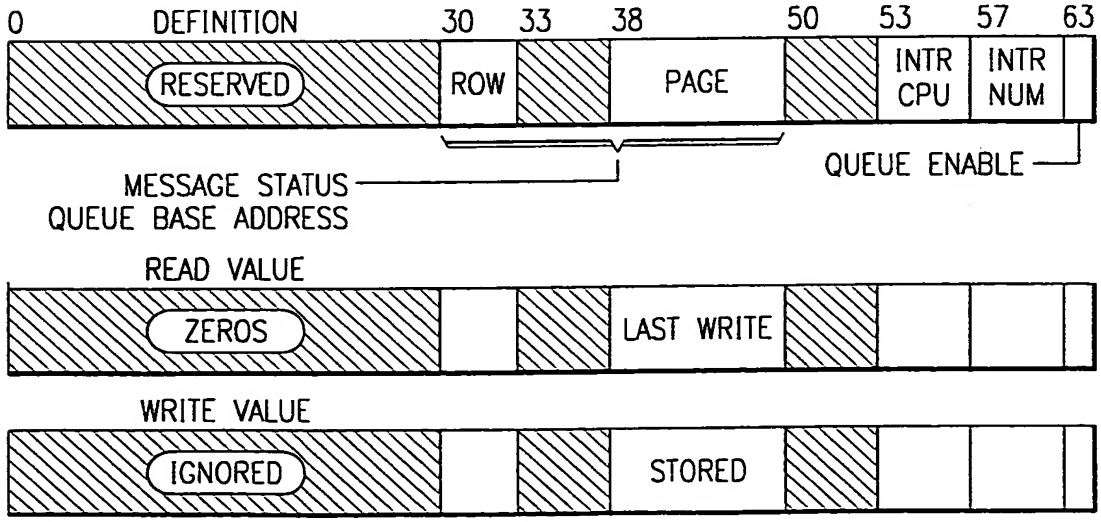


FIG. 9

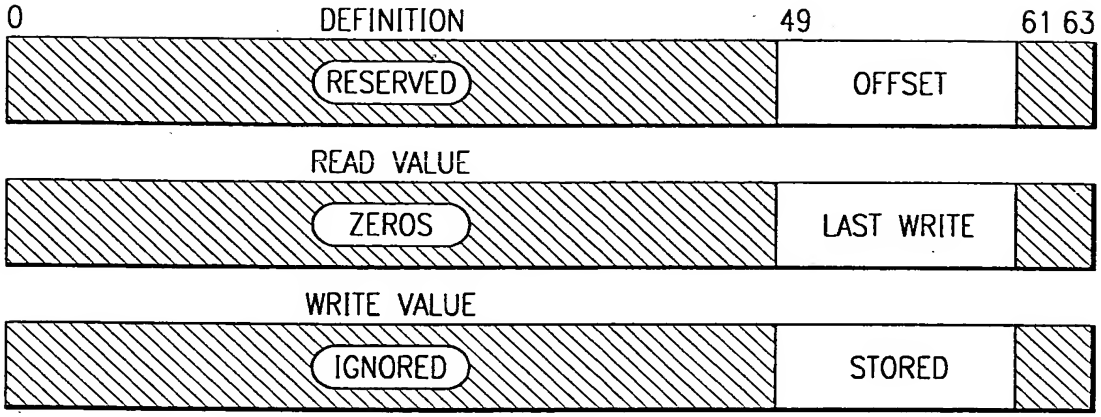


FIG. 10

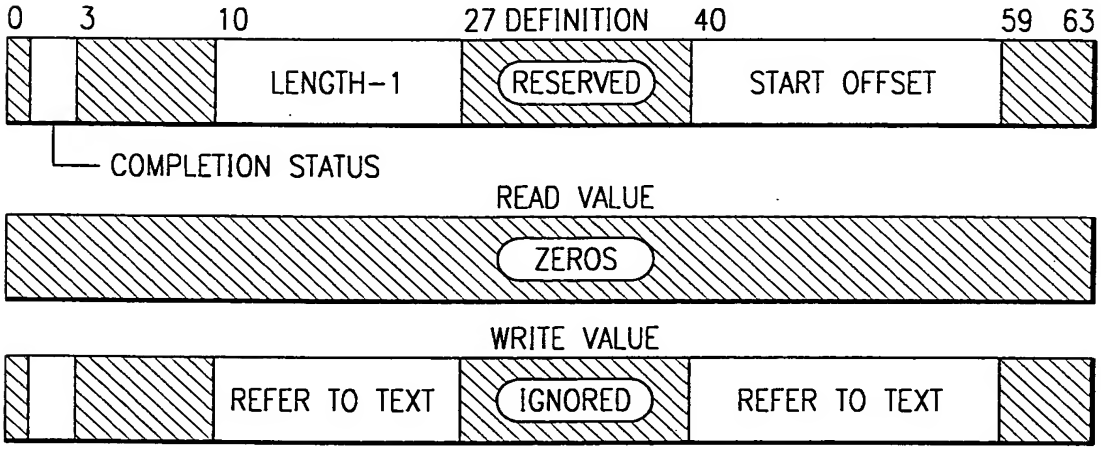


FIG. 11

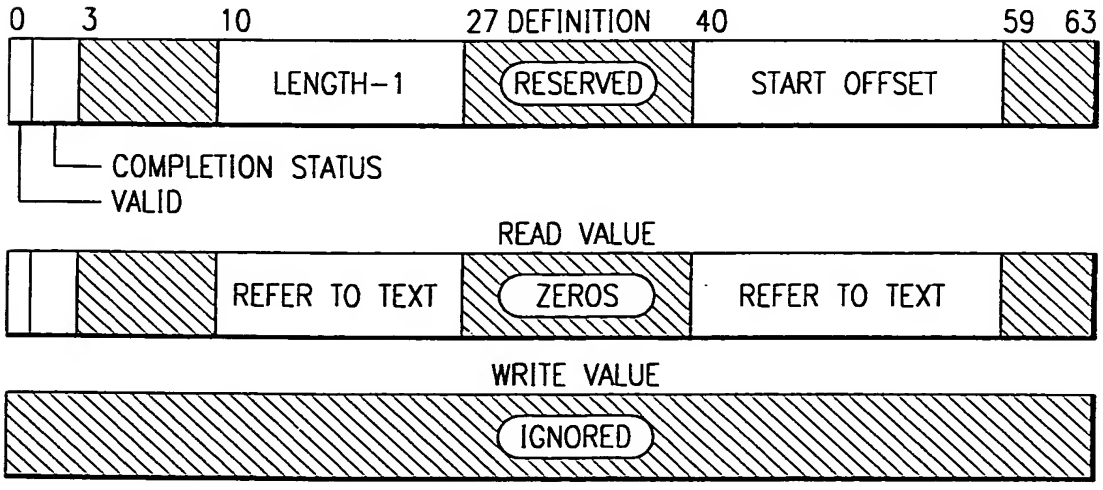


FIG. 12

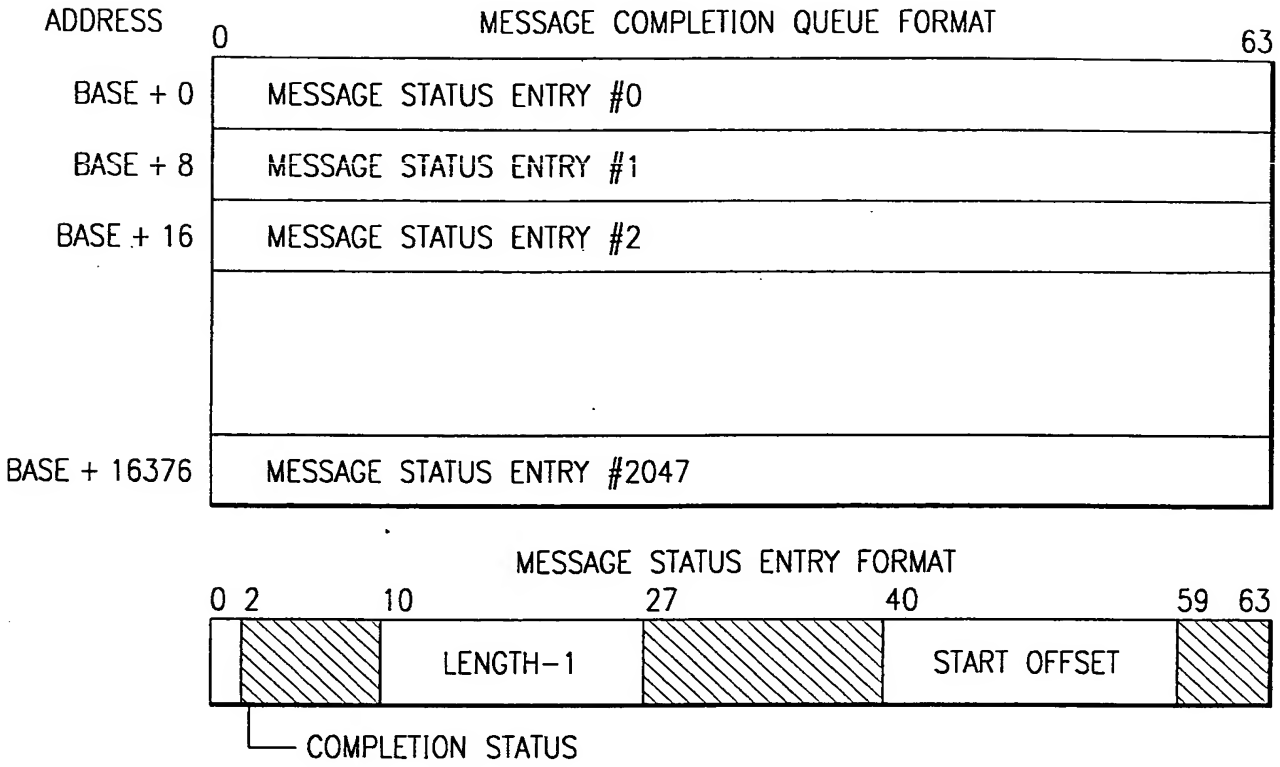
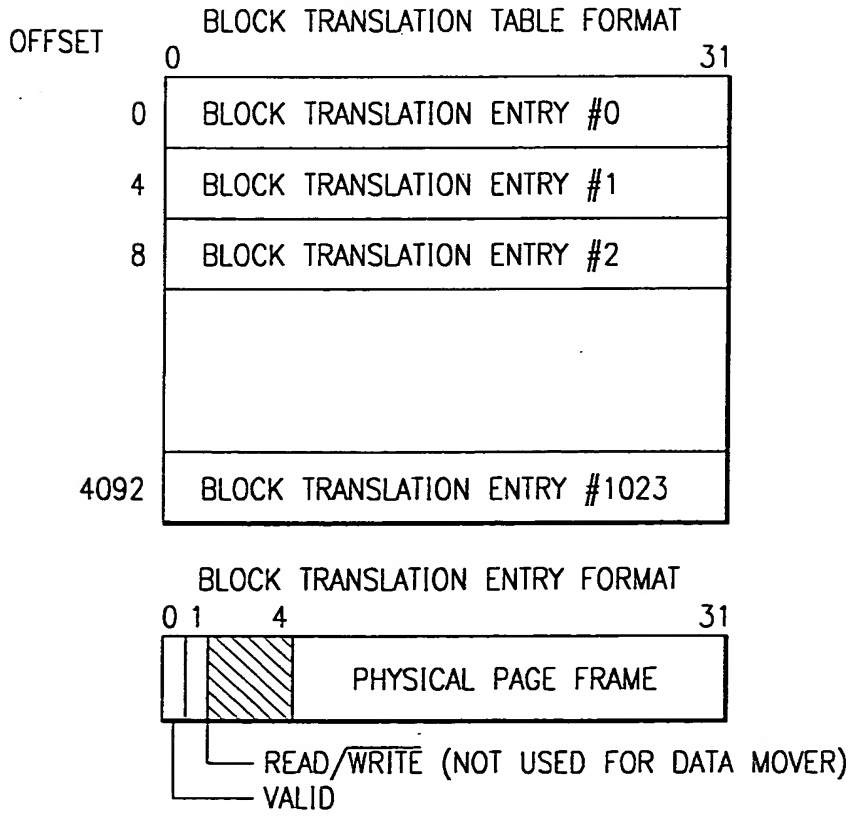

ADDRESS
MESSAGE COMPLETION QUEUE FORMAT
0
63
BASE + 0
MESSAGE STATUS ENTRY #0
BASE + 8
MESSAGE STATUS ENTRY #1
BASE + 16
MESSAGE STATUS ENTRY #2
BASE + 16376
MESSAGE STATUS ENTRY #2047
MESSAGE STATUS ENTRY FORMAT
0 2
10
27
40
59 63
LENGTH-1
START OFFSET
COMPLETION STATUS

FIG. 13


OFFSET
BLOCK TRANSLATION TABLE FORMAT
0
31
0
BLOCK TRANSLATION ENTRY #0
4
BLOCK TRANSLATION ENTRY #1
8
BLOCK TRANSLATION ENTRY #2
4092
BLOCK TRANSLATION ENTRY #1023
BLOCK TRANSLATION ENTRY FORMAT
0 1
4
31
PHYSICAL PAGE FRAME
READ/WRITE (NOT USED FOR DATA MOVER)
VALID

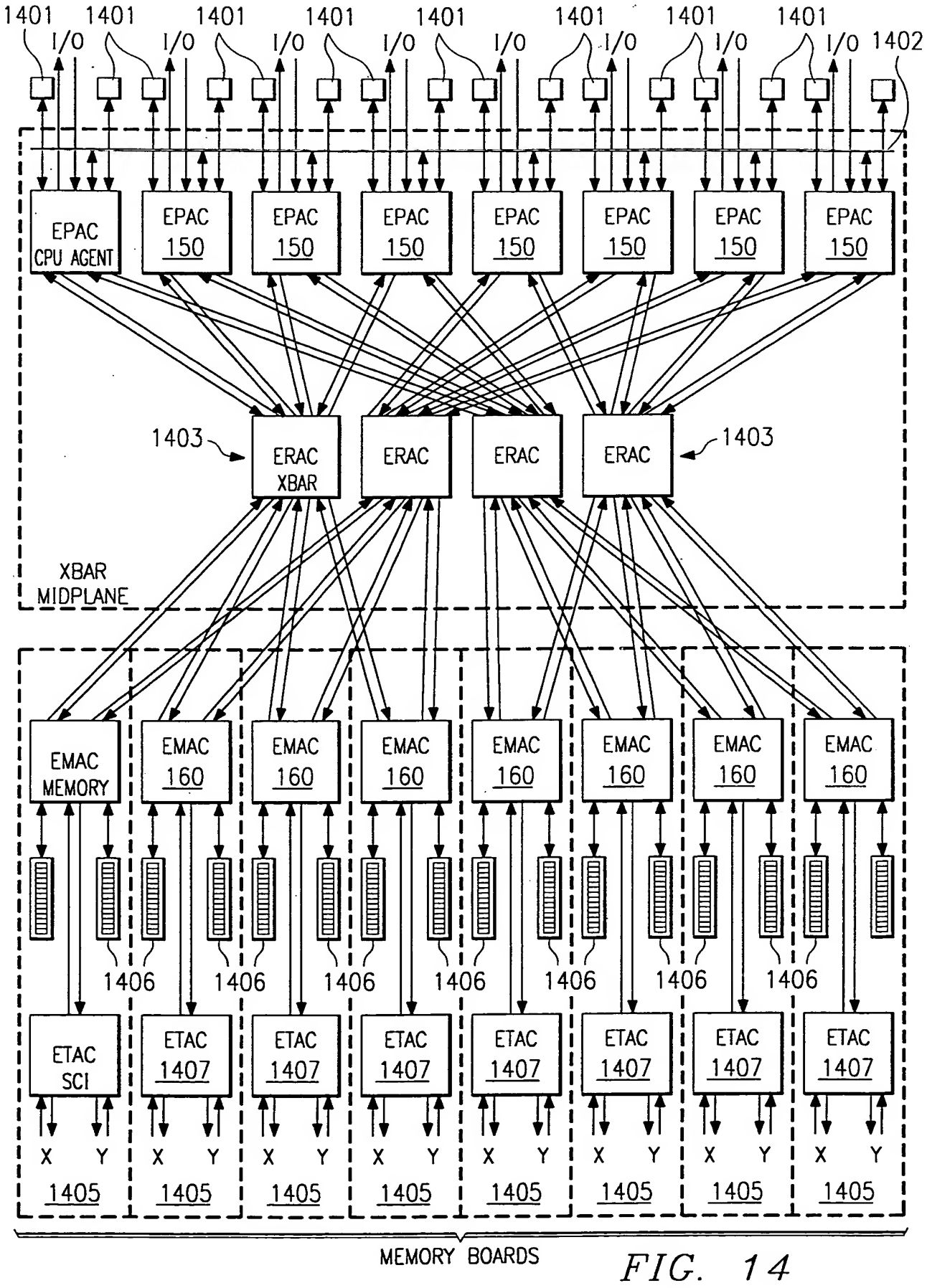

1401
I/O
1402
EPAC
CPU AGENT
EPAC
150
1403
ERAC
XBAR
ERAC
XBAR
MIDPLANE
EMAC
MEMORY
EMAC
160
1406
ETAC
SCI
ETAC
1407
X
Y
1405
MEMORY BOARDS

FIG. 14

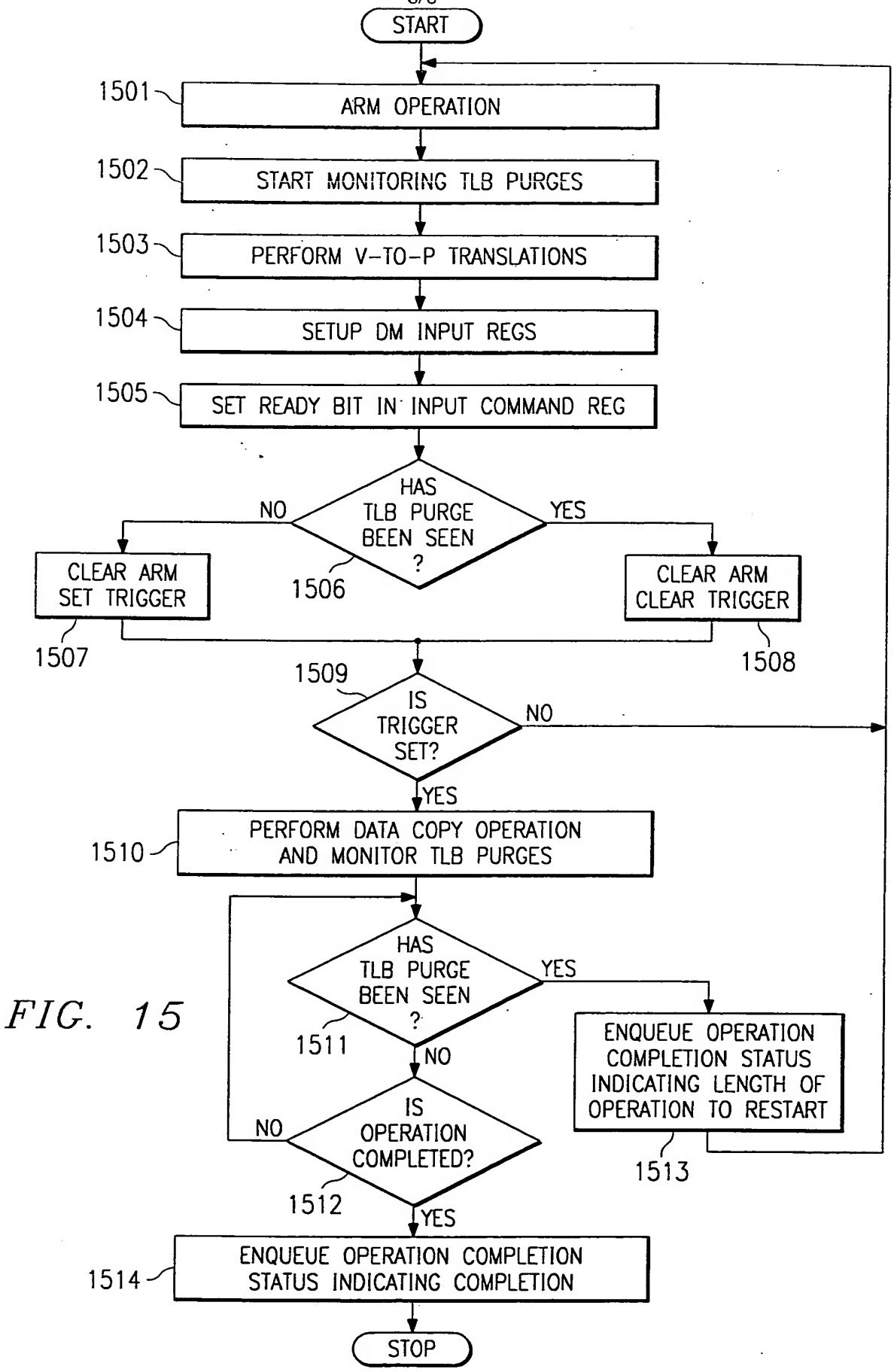

START
1501
ARM OPERATION
1502
START MONITORING TLB PURGES
1503
PERFORM V-TO-P TRANSLATIONS
1504
SETUP DM INPUT REGS
1505
SET READY BIT IN INPUT COMMAND REG
HAS TLB PURGE BEEN SEEN ?
1506
NO
YES
CLEAR ARM SET TRIGGER
1507
CLEAR ARM CLEAR TRIGGER
1508
1509
IS TRIGGER SET?
NO
YES
1510
PERFORM DATA COPY OPERATION AND MONITOR TLB PURGES
HAS TLB PURGE BEEN SEEN ?
1511
YES
NO
ENQUEUE OPERATION COMPLETION STATUS INDICATING LENGTH OF OPERATION TO RESTART
1513
IS OPERATION COMPLETED?
1512
NO
YES
1514
ENQUEUE OPERATION COMPLETION STATUS INDICATING COMPLETION
STOP

FIG. 15